Establishing a New Benchmark in Quantum Computational Advantage with 105-qubit *Zuchongzhi* 3.0 Processor

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In the relentless pursuit of quantum computational advantage, we present a significant advancement with the development of *Zuchongzhi* 3.0. This superconducting quantum computer prototype, comprising 105 qubits, achieves high operational fidelities, with single-qubit gates, two-qubit gates, and readout fidelity at 99.90%, 99.62% and 99.18%, respectively. Our experiments with an 83-qubit, 32-cycle random circuit sampling on *Zuchongzhi* 3.0 highlight its superior performance, achieving one million samples in just a few hundred seconds. This task is estimated to be infeasible on the most powerful classical supercomputers, Frontier, which would require approximately 6.4×10^9 years to replicate the task. This leap in processing power places the classical simulation cost six orders of magnitude beyond Google's SYC-67 and SYC-70 experiments [Nature **634**, 328 (2024)], firmly establishing a new benchmark in quantum computational advantage. Our work not only advances the frontiers of quantum computing but also lays the groundwork for a new era where quantum processors play an essential role in tackling sophisticated real-world challenges.

INTRODUCTION

The quest for quantum computational advantage, a concept first coined by John Preskill, has been a central driving force in the field of quantum computing [1–9]. This term captures the pivotal moment when a quantum computer is capable of executing calculations that are beyond the reach of even the most advanced classical computers. In 2019, Google claimed that its quantum processor, Sycamore [4], had achieved this milestone, demonstrating its capabilities through an experiment on a problem known as random circuit sampling, which was deliberately designed to be intractable by classical systems. Random circuit sampling [10–12] involves the creation of quantum states by applying a series of random quantum gates, followed by measurement. This process has become a focal point of intensive research due to its capacity to underscore the computational superiority of quantum systems. Since that breakthrough, the field has been eager to extend

these results to larger systems and more complex tasks, striving to solidify the quantum advantage in computational tasks. Particularly in experimental settings, China's *Zuchongzhi* processor [2, 3, 13–16] has been in continuous competition with Sycamore, pushing the boundaries of what is achievable with quantum technologies. To date, the largest scale of random quantum circuit is achieved by Google with 67 qubits at 32 cycles (SYC-67) and 70 qubits at 24 cycles (SYC-70) [5].

In this work, we aim to challenge this record. We have developed *Zuchongzhi* 3.0, a more powerful superconducting quantum computer prototype, equipped with 105 qubits and exceptionally high-fidelity manipulation capabilities. The single-qubit gate, two-qubit gate, and readout fidelities are 99.90%, 99.62%, and 99.18%, respectively. Leveraging this prototype, our experiments utilize a significantly larger quantum circuit of 83 qubits at 32 cycles, thereby pushing the limits of current quantum hardware capabilities. On our *Zuchongzhi* 3.0, the task of obtaining one million samples is accomplished in just a few hundred seconds. It is a stark contrast to the estimated 6.4×10^9 years, required by the most formidable supercomputers of today, Frontier, to replicate this sampling endeavor. Compared to Google's latest experiment, SYC-67 and SYC-70 [5], the classical simulation cost of our 83-qubit, 32-cycle experiment is six orders of magnitude higher. Through this achievement, we establish a new benchmark in quantum computational advantage, which is essential for harnessing the full potential of quantum computing. Beyond this, our work opens avenues for investigating how increases in qubit count and circuit complexity can enhance the efficiency in solving real-world problems.

ZUCHONGZHI 3.0 QUANTUM PROCESSOR

Zuchongzhi 3.0 quantum processor marks a significant upgrade from its predecessor, *Zuchongzhi* 2.0, with a notable increase in both the quantity and quality of qubits. It now houses 105 Transmon qubits, arrayed in 15 rows and 7 columns, forming a two-dimensional rectangular lattice as depicted in Fig. 1. We conducted experiments with a maximum of 83 qubits selected from the processor.

One of the most significant advancements in *Zuchongzhi* 3.0 quantum processor is the enhancement of coherence time. This improvement is achieved through several key strategies. First, we optimize the circuit parameters of the qubits, including the capacitance and the Josephson inductance, to reduce sensitivities to charge and flux noise. Second, we optimize the electric field distribution by modifying the shape of the qubit capacitor pads, which minimizes surface dielectric loss. Third, the attenuator configuration in the wiring is upgraded to mitigate noise from room-temperature electronics, significantly improving the dephasing time. Finally, we update the chip fabrication procedure by lithographically defining base components made of tantalum on the top sapphire substrate and aluminium on the bottom sapphire substrate, which are then bonded together using an indium bump flip-chip technique. This approach reduces the contamination at the interface and enhances the relaxation time of qubits. As a result, we improve the relaxation time (T_1) to 72 μs and the dephasing time ($T_{2,CPMG}$) to 58 μs.

The calibration processes for single-qubit gates and iSwap-like gates are similar to those employed in the *Zuchongzhi* 2.0. Due to advancements in coherence time, the average Pauli error for single-qubit gates(e_1) and iSwap-like gates(e_2) has been reduced to 0.10% and 0.38% respectively (as depicted in Fig. 2 (a) and (b)), when all gates are applied simultaneously.

The performance of readout is another significant advancement in the *Zuchongzhi* 3.0. To achieve fast readout with high fidelity, we increased the coupling strength between qubits and readout resonators to approximately 130 MHz and tuned the linewidths of the readout resonators to about 10 MHz. However, the increased coupling strength and linewidth result in a decrease in relaxation time. To address this, we optimized the design of the bandpass filter for dispersive qubit measurement, protecting the qubit from the Purcell effect.

Additionally, before each sampling task, we perform three rounds of measurement and apply the corresponding single-qubit gate to reset the qubit to the state $|0\rangle$. This method reduces the impact of thermal noise on state preparation and shortens the duration of each sampling. After these optimizations, the average readout error across 83 qubits has been suppressed to 0.82% (as depicted in Fig. 2 (c)).

LARGE-SCALE RANDOM CIRCUIT SAMPLING

After the initial calibration, we proceed with random quantum circuit sampling to evaluate the overall performance of the quantum processor. The random quantum circuit is designed in accordance with the method outlined in Ref. [17] to widen the performance gap between quantum computing and classical simulation. Notably, the two-qubit iSWAP-like gates within each layer of two-qubit gates are applied following a specific pattern, denoted by A, B, C, and D, as illustrated in Fig. 3 (a), and are executed in the sequence of ABCD-CDAB in each cycle. The single-qubit gates in each cycle are selected at random from the set $\{\sqrt{X}, \sqrt{Y}, \sqrt{W}\}$.

Verifying the fidelity of the full random quantum circuit is challenging due to the inability to simulate its ideal output classically. To address this, patch circuits are utilized for the verification of large-scale random quantum circuits. These patch circuits are crafted by selectively removing a portion of the two-qubit gates between the patches. The entire circuit can be divided into two independent segments, termed as 2-patch, or into four segments, known as 4-patch. The more divisions made, the more feasible the simulation becomes; however, the anticipated fidelity slightly increases due to the reduction in the number of two-qubit gates executed. We implement 2-patch, 4-patch, and the full version of the circuits, scaling from 12 to 32 cycles with 31 qubits each, and compute the linear XEB fidelities F_{XEB} for the respective output bitstrings.

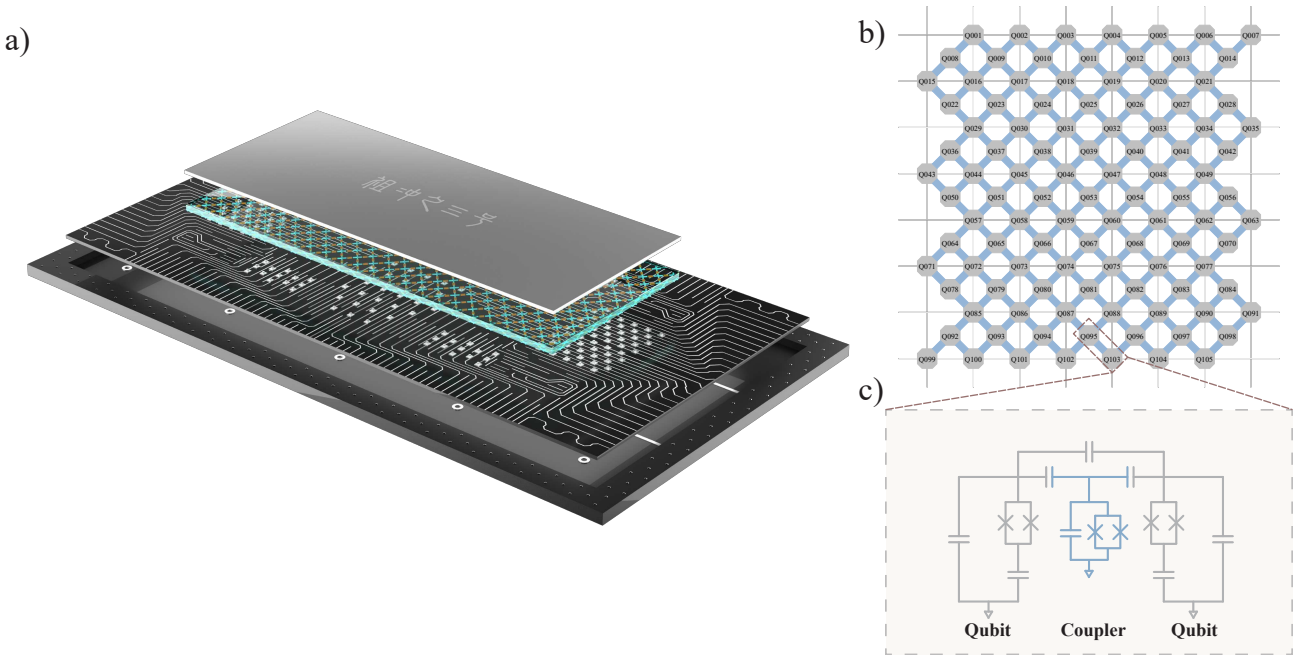

FIG. 1. ***Zuchongzhi* 3.0 quantum processor. a)** The illustration of the *Zuchongzhi* 3.0 quantum processor. The device consists of two sapphire chips integrated using a flip-chip technique. One chip integrates 105 qubits and 182 couplers, while the other is integrated with all the control lines and readout resonators. **b)** The topological diagram of qubits and couplers. Dark gray denotes qubits, light blue denotes couplers. **c)** Simplified circuit schematic of two qubits coupled via a coupler.

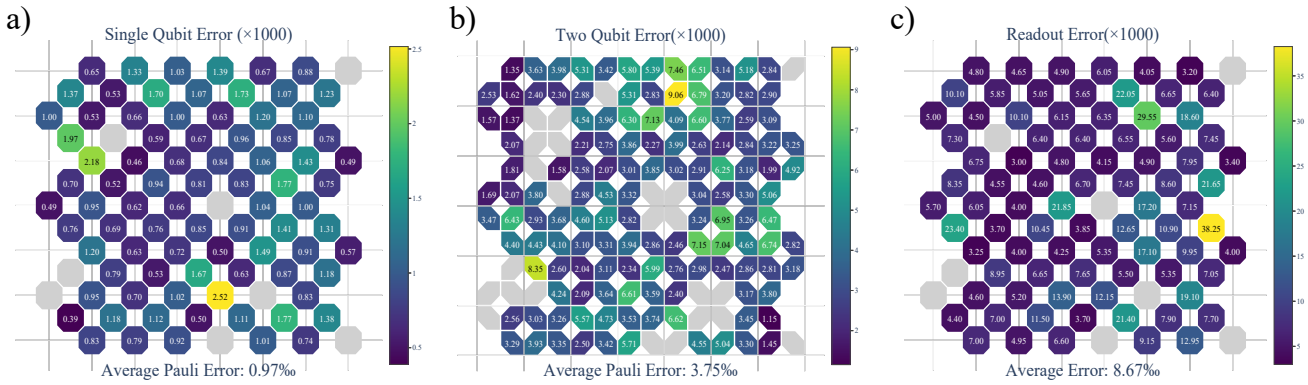

FIG. 2. **Gate and readout performance of the selected 83 qubits. a)** The single-qubit gate error, measured by XEB experiment, has an average value of 0.97‰ and a duration of 28 ns. **b)** The two-qubit gate error used in the experiment has an average value of 3.75‰ with a gate time of 45 ns. **c)** The average readout error rate is 8.67‰, achieved through active reset and 0-2 state readout, which improves readout fidelity while reducing the sampling interval to 400 μs. The provided values correspond to the simultaneous operation of all selected qubits. For the detailed calibration data on the complete set of 105 qubits, refer to the Supplemental Material.

The experimental results, as detailed in Fig. 3(b) (the results of 2-patch are displayed in Fig. S7 in Supplemental Material), reveal that the average fidelity ratios of the 4-patch circuit to the full circuit fidelity is 1.05. This high degree of correspondence indicates the effectiveness of the verification circuits in ensuring the fidelity of quantum computations.

Such an outstanding quantum processor allows us to run random circuit sampling on a larger scale than before. As shown in Fig. 3(c), we have achieved random circuit sampling of 83-qubit circuits with 12 to 32 cycles. For the largest full circuit featuring 83 qubits and 32 cycles, we have collected a total of approximately 4.1×10^8 bitstrings. To assess its fidelity, we also gathered corresponding bitstrings from 4-patch circuits, which exhibit an experimental fidelity of 0.030%, while the estimated fidelity stands at 0.033%. This high degree of correspondence indicates that, even at a large scale

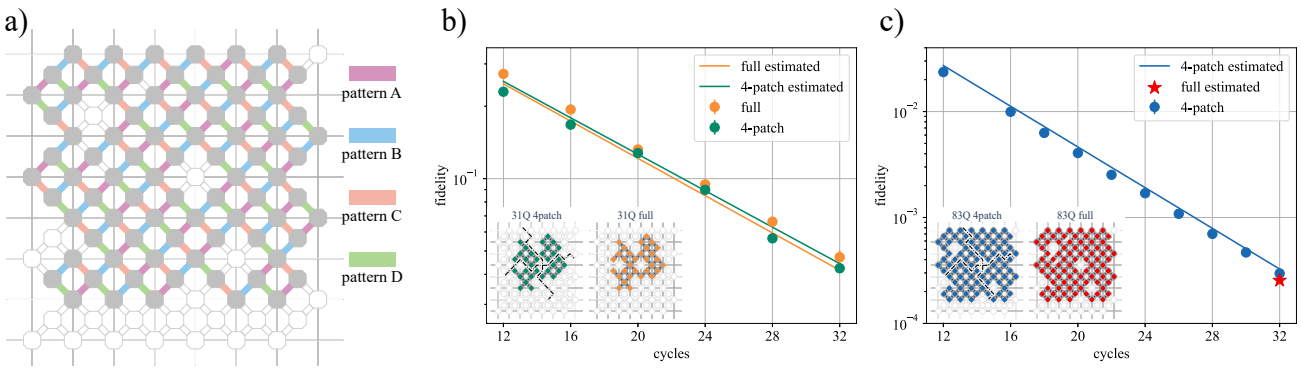

FIG. 3. **Experiment and estimate fidelity of random circuit sampling experiment for 31 qubits and 83 qubits. a)** The pattern diagram of the random circuit sampling experiment for 83 qubits. The iSWAP-like gates are selected from the patterns labeled A, B, C, and D, arranged in the sequence ABCDCDBA. The grey octagons denote functional qubits while purple, blue, orange, and green lines represent the iSWAP-like gates associated with the four pattern A,B,C,D respectively. Additionally, discarded qubits and couplers are indicated by empty octagons and lines. **b)** The green and blue dots respectively represent the experimental values of the 4-patch circuits and full circuits with 31 qubits over 12-36 cycles. The corresponding solid lines denote the estimated values for these circuits. The inserted topological diagram illustrates the specific configuration of 31 qubits. **c)** The blue dots and line correspond to the experimental and estimated values, respectively, of the 83-qubit 4-patch circuit. The red five-pointed star signifies the estimated value of the 83-qubit full circuit, where 410 million bitstrings are sampled. The inserted topological diagram depicts the specific configuration of 83 qubits.

TABLE I. **Estimated classical computational cost for different experiments.** The Frontier supercomputer boasts a theoretical peak performance of 1.685×10^{18} FLOPS. In our estimations, we presume a 20% FLOP efficiency and convert the machine FLOPS to single-precision complex FLOPS. We provide two scenarios: one with 9.2 PB of memory (the actual memory of Frontier) and another with 762.2 PB (combining Frontier's actual memory with all storage, which is an impractical situation).

Experiment	**Fidelity**	**Memory Constraint: 9.2PB**			**Memory Constraint: 762.2PB**		
		1 Amplitude (FLOP)	1 Million Noisy Samples (FLOP)	Runtime on Frontier	1 Amplitude (FLOP)	1 Million Noisy Samples (FLOP)	Runtime on Frontier
Sycamore-53-20	2.2×10^{-3}	7.2×10^{18}	6.5×10^{16}	1.6 s	5.9×10^{18}	6.1×10^{16}	1.5 s
Zuchongzhi-56-20	6.6×10^{-4}	9.3×10^{19}	2.2×10^{17}	5.3 s	1.0×10^{20}	1.5×10^{17}	3.6 s
Zuchongzhi-60-24	3.7×10^{-4}	3.2×10^{21}	1.6×10^{19}	384.0 s	3.0×10^{21}	2.3×10^{18}	55.2 s
Sycamore-70-24	1.7×10^{-3}	1.7×10^{25}	8.2×10^{25}	62.1 yr	3.2×10^{24}	1.4×10^{24}	1.1 yr
Sycamore-67-32	1.5×10^{-3}	8.2×10^{28}	4.7×10^{27}	3.6×10^{3} yr	1.3×10^{26}	9.6×10^{24}	7.2 yr
Zuchongzhi-83-32	2.5×10^{-4}	5.1×10^{31}	8.4×10^{33}	6.4×10^{9} yr	1.3×10^{29}	7.5×10^{31}	5.7×10^{7} yr

of qubits and high circuit depth, employing the discrete error model to estimate fidelity remains highly reliable. Consequently, we can estimate the fidelity of the full circuit with 83 qubits and 32 cycles to be 0.025%.

COMPUTATIONAL COST ESTIMATION

The current cutting-edge classical algorithm for simulating random quantum circuits is the tensor network algorithm [18–27]. We employ this method to evaluate the classical computational cost of our harderst circuit, featuring 80 qubits and 32 cycles. Considering memory constraints, we have examined the following two scenarios using the state of the art method [26, 27].

The first scenario involves capping the memory at 9.2 petabytes (PB), which is the memory size of the current most powerful supercomputer, Frontier. The estimated number of floating-point operations required to generate a million uncorrelated bitstrings with a fidelity of 0.025% from an 83-qubit, 32-cycle random circuit using a classical computer is 8.4×10^{33}. In contrast, the latest quantum computational advantage experiment by Google [5], SYC-67, has an estimated classical simulation complexity of 4.7×10^{27} for replicating the same number of bitstrings with fidelity that matches its experiment. Hence, the classical cost of simulating our most challenging random quantum circuit is six orders of magnitude higher than that of SYC-67. For our estimates, we utilize the specifications of the Frontier supercomputer, which boasts a theoretical peak performance of 1.685×10^{18} single precision FLOPs per second. We assume a 20% FLOP efficiency and take into account the low target fidelity of the simulation in the computational cost. Each single precision complex FLOP necessitates 8 machine FLOPs. Under these conditions, the projected time for classical simulation of our

most challenging random quantum circuit is 6.4×10^9 years using the current most powerful supercomputer, Frontier.

The complexity of tensor network algorithms is influenced by memory limitations, and we have further contemplated the scenario of virtually unlimited memory as an estimated lower bound for the sampling cost, although this situation is already unrealistic. By setting the memory limit to over 762.2 PB (considering both memory and total storage of Frontier as part of the memory), we estimate the number of floating-point operations needed to generate a million uncorrelated bitstrings of the same fidelity from our most challenging 80-qubit, 32-cycle random circuit remains high, at 7.5×10^{31}. Consequently, the estimated classical simulation time is an immense 5.7×10^7 years, which underscores the robustness of our quantum advantage.

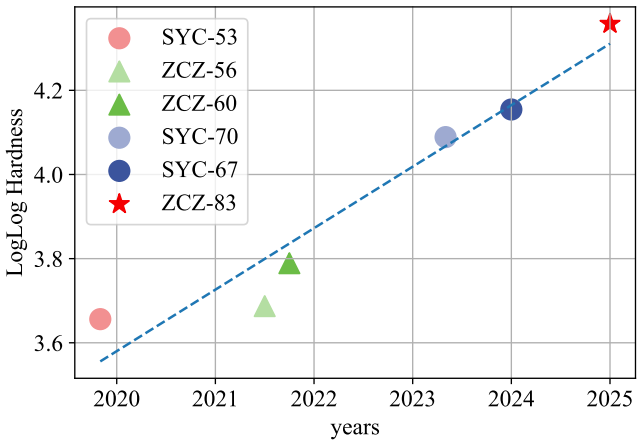

FIG. 4. **Progress on random circuit sampling.** The evolution of the time complexity in random circuit sampling experiments. The dotted line illustrates the pattern of doubly-exponential growth. SYC and ZCZ respectively denote the Sycamore and *Zuchongzhi* processors.

CONCLUSION

The *Zuchongzhi* 3.0, an advanced superconducting quantum computer prototype with its 105 qubits and exceptional operational fidelities, not only ups the ante in terms of the number of qubits but also enhances the precision of quantum manipulation. This dual advancement is key to expanding our quantum computing capabilities. Based on this robust platform, we have successfully executed a larger scale random circuit sampling than previously achieved by Google [5], further widening the gap in computational capabilities between classical and quantum computing. Our work advances the discourse on quantum computing by providing empirical evidence of the technology's potential to revolutionize computational tasks. It serves as both a testament to the progress in quantum hardware and a foundation for practical applications. Scaling up in qubits and circuit complexity enhances our capacity to address sophisticated challenges in optimization [28], machine learning [29–31], and drug discovery.

Funding: This research was supported by the Innovation Program for Quantum Science and Technology (Grant No. 2021ZD0300200), Anhui Initiative in Quantum Information Technologies, the Special funds from Jinan Science and Technology Bureau and Jinan high tech Zone Management Committee, Shanghai Municipal Science and Technology Major Project (Grant No. 2019SHZDZX01), and the New Cornerstone Science Foundation through the XPLORER PRIZE. M. Gong was sponsored by National Natural Science Foundation of China (Grants No. T2322024), Shanghai Rising-Star Program (Grant No. 23QA1410000) and the Youth Innovation Promotion Association of CAS (Grant No. 2022460). H.Huang was supported from the National Natural Science Foundation of China (Grant No. 12274464), and Natural Science Foundation of Henan (Grant No. 242300421049). C.Zha was sponsored by Shanghai Science and Technology Development Funds (Grant No. 23YF1452500) and the China Postdoctoral Science Foundation (Grant No. 2023M740964). J.Li was supported by the Key-Area Research and Development Program of Guangdong Province (2020B0303060001). **Author contributions:** X.Z., and J.-W.P. conceived the research. Y.Z., X.Z., and H.H. provided the theoretical calculations. D.G., D.F., and C.Z. designed and perform the experiment. C.P. conceived the electronics and software. All authors contributed to the discussion of the results and the development of this work. X.Z. and J.-W.P. supervised the whole project.

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Supplemental Material for "Establishing a New Benchmark in Quantum Computational Advantage with 105-qubit *Zuchongzhi* 3.0 Processor"

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(Dated: December 17, 2024)

I. DEVICE INFORMATION

A. Quantum processor

Zuchongzhi 3.0 is a superconducting programmable quantum processor, comprising of 105 Transmon qubits [1] and 182 tunable couplers [2], arranged in 15 rows and 7 columns, as depicted in the main text. Each qubit exhibits an anharmonicity of approximately -230 MHz, with a control line for XY gates and iSWAP-like gates, except for the qubits Q_{022} and Q_{037}, whose frequencies are non-tunable. For the precise measurement of qubit states, a readout resonator is individually coupled to each qubit, and shares a bandpass filter with the other six resonators to suppress the Purcell effect. Additionally, each coupler is equipped with a control line, allowing for the fine-tuning of the coupling strength between neighboring qubits.

The fabrication process closely follows that of *Zuchongzhi* 2.0 [3], with a key enhancement being the employment of tantalum film for the patterning of base wirings on the top substrate.

B. Control electronics and Cryogenic wiring

The experimental wiring setup for qubit/coupler controls and frequency-multiplexed readouts is shown in Fig. S1.

The cryogenic wiring used in this experiment is a modular high-density cable system. Above the mixture chamber plate, the dilution system consists of 2×12 semi-rigid cables as-

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sembled in a modular fashion. In the mixture chamber plate, modular noise filters and thinner flexible phase-stable cables are used to ensure optimal signal transmission and noise reduction. Each layer is also equipped with modular attenuators, allowing for signal and noise damping. The modular design and the reduced diameter of cables allow for a large number of cables to be installed within the refrigerator.

We combined the XY control lines and Z control lines at room temperature using combiners before connecting them to the cables inside the refrigerator, which further reduced the number of cables needed for the quantum chip. The refrigerator used in this experiment is equipped with a total of 504 cables, of which 332 cables were used in this experiment.

The control and readout setup employed in this experiment is the same as that of *Zuchongzhi* 2.0. However, we have also made significant upgrades: the near-quantum-limited amplifier for readout has been replaced with a traveling-wave parametric amplifier (TWPA) [4, 5], and the configuration of the circulators has been correspondingly optimized. Additionally, a specific bandpass filter is added in front of the room-temperature amplifier to prevent the TWPA pump signal from infiltrating the ADC modules.

The room temperature electronic equipment in this experiment includes 407 DAC channels, 15 ADC modules, and 21 microwave source channels. The reduction in the number of microwave source channels is due to the use of microwave amplification modules, which allow a single microwave source channel to provide the local signals needed for 32 DAC channels.

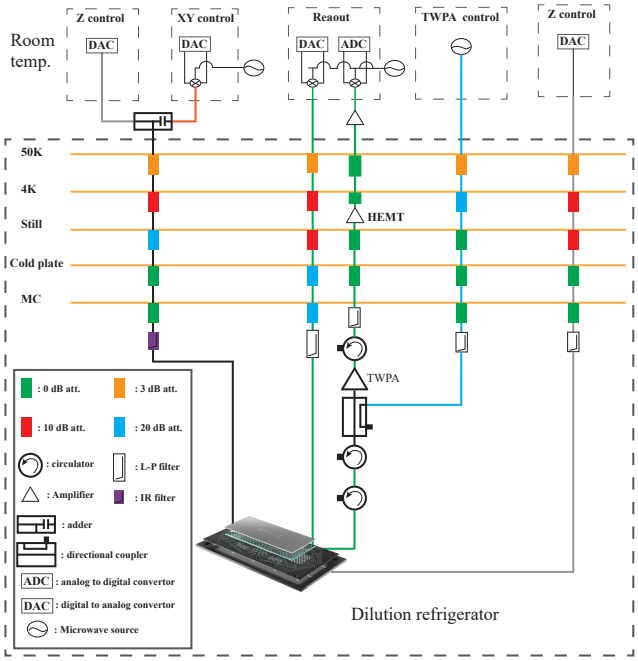

FIG. S1. **The schematic diagram of control electronics and wiring configuration**. Within the dilution refrigerator, attenuators and filters are installed at various plate to reduce the amplitude and noise of signals. For signal amplification, we employ Traveling-Wave Parametric Amplifiers (TWPAs), High Electron Mobility Transistors (HEMTs), and room-temperature amplifiers to enhance the readout signals. Directional couplers and circulators are utilized to prevent unwanted microwave coupling. At room temperature, the Z control pulse and XY control microwave are combined via an adder and the microwave sources are employed to pump the TWPA.

II. SYSTEM CALIBRATION

The basic calibration encompasses a suite of experiments designed to ascertain the fundamental properties of the quantum processor, including readout frequencies, the responses of qubit frequencies to flux bias, XY crosstalk, and coherence times. The fundamental properties of the 105-qubit processor are list in the Fig. S2.

The calibration procedures for *Zuchongzhi* 3.0 are analogous to those of *Zuchongzhi* 2.0, as detailed in our previous work [3], and thus will not be reiterated in this manuscript. Instead, we will delve into the distinctive method applied in our random circuit sampling experiment.

A. Idle Frequency Configuration for 83 qubits

In our pursuit of quantum computational advantage with the processor's fundamental performance, we meticulously consider the fidelity of sampling, the complexity of the quantum circuits, and the inherent defects of both qubits and couplers. After a thorough evaluation, we have chosen a subset of 83 qubits for our random circuit sampling task, as shown in the main text. The other qubits are biased to their minimum frequencies to mitigate unwanted interactions with the active qubits. Additionally, we have turned off the coupling between the active qubits and those that are biased with couplers tuning.

For the avtive 83 qubits, we optimize the idle and interaction frequency arrangements, leveraging the basic calibration results of 83 qubits. During the idle frequency optimization, several critical factors are taken into account: coherence, two-level-system (TLS), residual coupling between qubits, XY-crosstalk, and Z pulse distortions. These considerations have enabled us to determine the optimal idle frequency configuration, as depicted in Fig S4 (b).

However, we observe that the T_1s performance at the idle frequencies sometimes exhibit significant variations throughout the experiment, attributed to the effects of the TLS. When qubits are subject to the influence of the TLS, we measure their T_1s near the idle frequencies and subsequently retune the idle frequencies of the affected qubits to mitigate the impact of the TLS.

With the stable and high-performance idle frequency configuration for 83 qubits, we proceed to calibrate the gate operations and readout processes employed in the random sampling experiment.

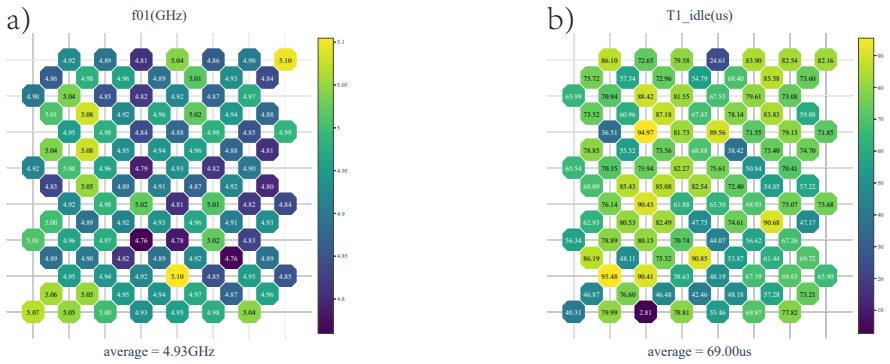

FIG. S2. **Typical parameter distribution of the 105-Qubit in the *Zuchongzhi* 3.0**

B. Gate and Readout Calibration

1. *Single-Qubit Gate Calibration*

After the highly precise calibration of the diving frequency, driving amplitude, and drag alpha for the single-qubit gate, we are enabled to realize a single-qubit gate with remarkably low control errors. However, the close adjacency of qubit control lines engenders crosstalk within the control signals. Consequently, this crosstalk induces discrepancies in single-qubit gate when they are carried out simultaneously as compared to when they are performed individually. Although the XY-crosstalk can be ameliorated by modulating the difference in idle frequencies between qubits, This concomitantly imposes more stringent constraints on the layout of idle frequencies, which becomes especially prominent as the qubit scale expands.

To resolve this issue, we apply crosstalk cancellation signal to the compensated qubit Q_c, according to the driving waveform of the crosstalk qubit Q_x. The frequency of the cancellation waveform is the same as that of the driving waveform, while the amplitude is determined by the amplitude of the driving waveform, denoted as $A_c = A_x * \alpha_{cx}$, where α_{cx} represents the output ratio between the two channels. We obtained the initial value of α_{cx} by driving Q_c with the frequency of Q_c on the control lines of both the Q_c and Q_x respectively, and then measuring and comparing the periods of the corresponding Rabi oscillations utilizing the circuit depicted in the upper left corner of Fig. S3 (a). The additional phase δ_ϕ of the cancellation waveform is extracted from the circuit shown in the upper right corner of Fig. S3 (a). We scan additional phase δ_ϕ of the compensation microwave to observe the probability of Q_c remaining in state $|0\rangle$. The phase corresponding to the point with the highest probability is the optimal value. Subsequently, the precise value of α_{cx} is determined by Fine scan α_{cx}. The bottom part of Fig. S3 (a) illustrates the comparison between the cases with and without XY-crosstalk correction, where the average Pauli error of Cross-Entropy Benchmarking (XEB) [6] is reduced from 1.78% to 0.99%.

2. *Readout Calibration*

We use a 0-2 readout method to improve the readout fidelity [7], where an X_{12} gate is applied to the qubit prior to measurement, preparing the qubit in either the $|0\rangle$ or $|2\rangle$ state. This method effectively reduces decoherence errors during readout but results in an increased sampling interval.

To solve this issue, we implement an electronics-based active reset procedure [8, 9]. Specifically, the qubit state is read at the beginning or end of the experiment, and a corresponding gate (denoted as CONDX) is subsequently applied based on the measured state. For the 0-2 readout method, when the qubit is measured in the $|0\rangle$ state, CONDX is the identity (I) gate, and when the qubit is measured in the $|1\rangle$ state, CONDX consists of the combination of $X_{12} + X_{01}$ gates. In Fig. S3 (b), the top graph represents the process of acitve reset, and the bottom graph is the CDF diagrams of readout error with and without active reset. Under the condition of sampling interval = $400\mu s$, the readout error is reduced from 2.21% to 0.93% after applying active reset.

To further improve the fidelity of the active reset process, we partition the phase space using a support vector machine (SVM) technique. However, this step introduces a small degree of initial state preparation errors, which will be calibrated in Section II C 4.

The readout error is obtained by simultaneously preparing all qubits in either $|0\rangle$ or $|1\rangle$, and measuring the corresponding error rates. To reduce correlated readout errors, we carefully tune the qubit frequencies during the readout process to avoid frequency collisions, achieving relatively low readout error rates.

3. *Two-Qubit Gate Calibration*

The calibration and characterization process for the iSWAP-like gate adopted in this paper can be primarily summarized into the following steps:

1. We determine the swap frequency using an optimization

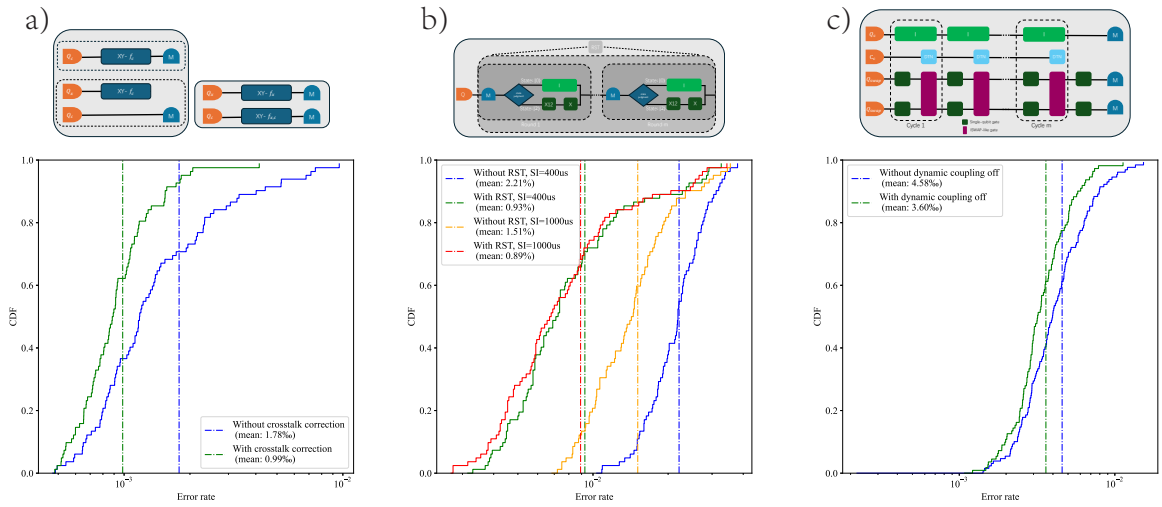

FIG. S3. **XY-crosstalk correction, active reset, dynamic coupling-off correction.** **a)** Top: The circuit diagram on the left is used for the rough correction of the amplitude correction coefficient of the cancellation signal, while the circuit diagram on the right is used for the fine correction of the amplitude correction coefficient and phase of the cancellation signal. Bottom: CDF diagrams of single-qubit gate Pauli error with and without XY-crosstalk correction. **b)** Top: The schematic diagram of the active reset circuit. In our experiment, we carried out three rounds of active reset to ensure the qubit is reset back to the $|0\rangle$ state. Bottom: CDF diagrams of readout error with and without active reset. **c)** Top: Circuit diagram of dynamic coupling-off. Bottom: CDF diagrams of two-qubit gate Pauli error with and without dynamic coupling-off. The vertical dotted lines in **a)**, **b)** and **c)** represent the average value.

algorithm, which primarily incorporates the T_1, T_2 of the qubits at the swap frequency, as well as frequency collisions with neighboring qubits.

2. With a fixed total gate time of 45ns, we can scan the two-dimensional map of the coupling strength g and the detuning frequency DTN required for aligning the frequencies of the two qubits. Here, we fix the detuning of one qubit and scan the detuning of the other to obtain initial values for g and DTN.

3. The pulse distortion for the qubits is calibrated based on the initial detuning frequency DTN [10].

4. We refine the optimal values of the coupling strength g and the detuning parameter DTN. To enhance the sensitivity of the parameters, we meticulously adjust g and DTN by employing a sequence of odd-numbered iSWAP-like gates.

5. Due to periodic variations of two level system (TLS) and frequency collisions, the swap frequency optimized by the optimizer requires fine-tuning. We rescan the swap frequency, targeting the SPB value, to avoid frequency conflicts and TLS effects.

6. We perform a scan to determine the dynamic coupling-off point of neighboring qubits. During the implementation of the iSWAP-like gate, the relevant two qubits are detuned, which can lead to their unintended recoupling with other neighboring qubits. The recoupling can cause significant state leakage if their idle or operational frequencies are in close proximity. Therefore, we apply a DTN to the neighboring coupler and scan for the optimal coupling-off point during gate operation. The specific circuit diagrams and the comparison of the two-qubit gate Pauli error with and without dynamic coupling-off are shown in Fig. S3 (c).

7. We optimize the rising edge time of qubits and couplers. At this step, we scan the rising edge time of the waveforms of two qubits and the coupler. Similarly, we take the value of SPB as the benchmark to determine the optimal rising edge time.

8. We employ XEB method to benchmark the parallel iSWAP-like gates performance.

The calibration results for the selected 83 qubits are presented in the Fig. S4, and the detailed statistical data are presented in S1.

C. Fine Calibration for Random Circuit Sampling Experiment

Following the calibration of gate operations and readout processes, we achieve a high XEB fidelity for these operations. However, the quantum circuits used in the random circuit sampling experiment, which are executed in the sequence of ABCDCDAB, differ from the circuits employed in the XEB method, which are executed in the sequence of A. It leads to a deviation between experimental fidelity and predicted fidelity

Parameters	Mean	Median	Stdev.
Qubit maximum frequency (GHz)	5.039	5.028	0.071
Qubit idle frequency (GHz)	4.914	4.920	0.070
Qubit anharmonicity (MHz)	-229.4	-228.7	3.8
Readout drive frequency (GHz)	6.408	6.391	0.100
T_1 at idle frequency (μs)	71.6	73.4	13.8
T_2^{CPMG} at idle frequency (μs)	57.8	56.5	15.3
Readout $e_{\|0\rangle}$ simultaneous (‰)	4.97	3.70	5.32
Readout $e_{\|1\rangle}$ simultaneous (‰)	12.37	8.90	8.99
1Q XEB e_1 simultaneous (‰)	0.97	0.88	0.41
1Q XEB e_1 purity simultaneous (‰)	0.63	0.54	0.27
2Q XEB e_2 simultaneous (‰)	3.75	3.27	1.60
2Q XEB e_2 purity simultaneous (‰)	3.59	3.35	1.50

TABLE S1. **Summary of system parameters of the 83-qubit subset.**

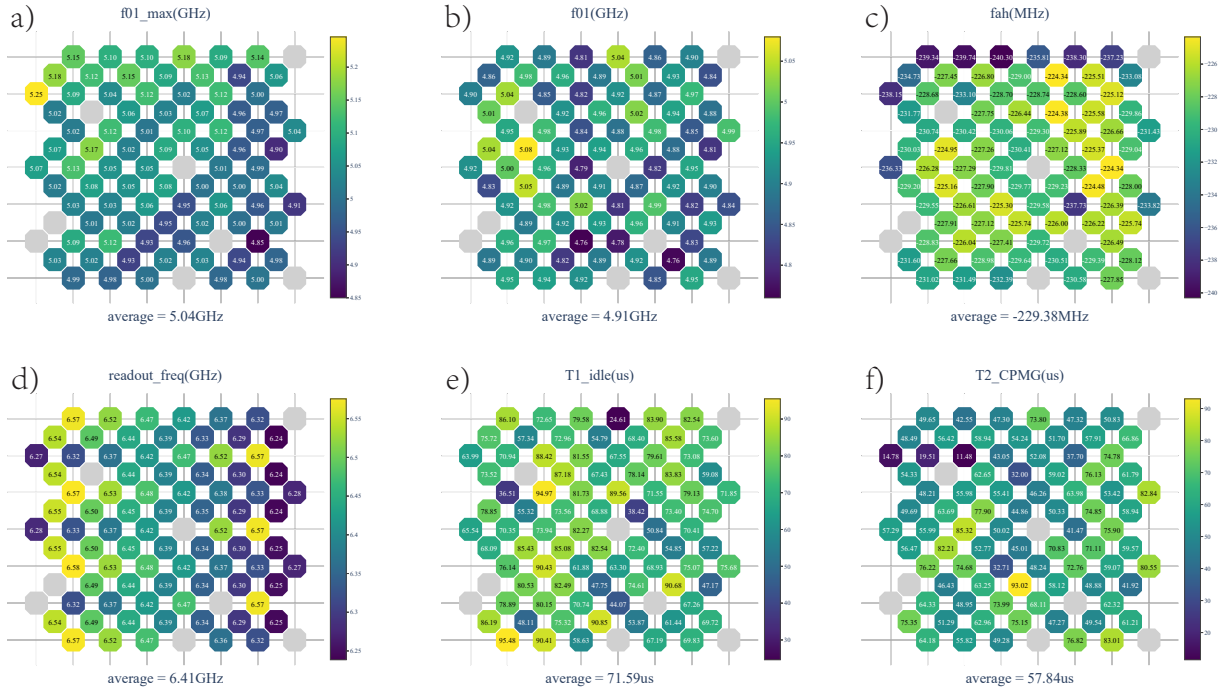

FIG. S4. **Typical parameter distribution of the 83-qubit subset in the *Zuchongzhi* 3.0**

Certain factors, including idle gate fidelities, pulse distortion of couplers, and state preparation errors, are not captured in the fidelities of XEB circuits but are reflected in the fidelities of the random circuits. Consequently, it is imperative that we calibrate for these factors to ensure the accuracy of random circuit sampling experiment.

It should be noticed that to closely align the calibrated effects of Z pulse crosstalk, dynamic coupling-off, and residual coupling with neighboring qubits, to those in the random circuit sampling experiment, we apply all waveforms to the qubits and couplers in the pattern during the calibration process.

1. 4-patch calibration

The modular high-density cable configuration introduces significant Z pulse crosstalk between two Z control lines, resulting in substantial pulse distortion due to crosstalk. The effect of Z pulse crosstalk can be mitigated by aligning calibration conditions as closely as possible with experimental conditions. However, the distortion associated with pulse crosstalk cannot be effectively reduced through standard calibration methods.

Due to the residual pulse distortion, the sequence of the pattern substantially alters the actual pulses applied to qubits and couplers during iSWAP-like gate operations. It leads to a dis-

crepancy between the unitary matrix of the calibrated iSWAP-like gates and the one observed in the sampling experiment.

We employ the 4-patch calibration method, as detailed in the *Zuchongzhi* 2.1 [11], to optimize the parameters of the iSWAP-like gate used in our sampling experiment. This optimization is based on the original gate parameters derived from two-qubit XEB calibration. Figure S5 illustrates a comparison of the parameters before and after the 4-patch calibration. The 4-patch calibration brings the calibrated parameters closer to their actual values and aligns the experimental fidelities more closely with the predicted fidelities. Consequently, in all subsequent random circuit sampling experiments, unless otherwise specified, we perform the 4-patch calibration.

2. *Idle Gate Benchmarking and Calibration*

In the random circuit sampling experiment, we divided all the iSWAP-like gates into 4 groups of patterns and executed them alternately in a specific order. For instance, the order adopted in our paper is ABCDCDAB. As not all 83 qubits are engaged in every iSWAP-like gate pattern, certain qubits are designated to execute idle gates in various pattern. The idle gate time is 45 ns, which is the same as the total time of iSWAP-like gates. During the idle gates, the qubits are affected not only by their own decoherence but also by Z-crosstalk, dynamic coupling-off, and residual coupling with neighboring qubits. Consequently, we need to calibrate the errors of the idle gates in each pattern.

Firstly, we benchmark the fidelity of the idle gates utilizing the quantum circuit as shown in Fig. S6 (a), adopting a method akin to that used in single-qubit XEB experiments. Fig. S6 (b) illustrates that the fidelity of the idle gate significantly deviates from the fidelity estimated by SPB, due to the Z crosstalk, dynamic coupling-off, and residual coupling with neighboring qubits.

To address the influence of the coupling with neighboring qubits, we re-scan for dynamic coupling-off and interaction frequencies. The qubit frequency shift can be corrected by applying Z gates as compensation. Balancing time and precision, we target the value of XBE under 100 cycles and scan the amplitude of Z gate to determine the optimal compensation amplitude.

3. *Calibration of Coupler Distortion*

In our two-qubit gate calibration experiments, we achieve a notably high gate fidelity, even in the absence of corrections for pulse distortion of the couplers. However, during the random circuit sampling experiments, the experimental fidelity of each cycle is slightly lower than the fidelity predicted based on the number of gates. We hypothesize that this discrepancy arises because, in the two-qubit gate calibration, the relatively deep circuit leads to a stabilization of the coupler's pulse distortion. This stabilization allows the two-qubit gates at various cycles to be effectively represented by the same unitary matrix. Conversely, in the random circuit sampling experiments, the comparatively shallow circuit and the alternating sequence of four patterns result in two-qubit gates at different cycles being represented by distinct unitary matrices.

According to our hypothesis, it is imperative to correct the pulse distortion of the couplers. Given that we cannot directly measure the frequency variation of the coupler, we rely on indirect detection through associated qubits. Analogous to the pulse distortion correction for qubits, we can obtain the frequency response of the detection qubits at various times after the Z pulse of the coupler ends. By leveraging the relationship between the detuning amplitude of the coupler and the frequency shift of the detection qubits, we can deduce the distortion of the actual coupler voltage inversely. Once the response functions at different times are determined, we apply the correction method outlined in Ref. [10] to rectify the distortion. With the corrected Z pulses for the couplers, the experimental fidelity in each cycle of the random circuit sampling experiments aligns closely with the predicted fidelity.

4. *Calibration of State Preparation Errors*

Following the calibration of the idle gates and correction of coupler distortions, a consistent deviation between experimental and predicted fidelities remains, independent of circuit cycle. We attribute this discrepancy to state preparation errors.

Since the effect of our current 02 readout reset scheme is based on the state of the qubit prior to the reset, the state preparation errors in the random circuit sampling process are different from those in the standard readout fidelity calibration. To achieve a more realistic estimate of the state preparation errors, we adopted the circuit shown in Fig. S6 (a) to calibrate the state preparation error correction factor. In this circuit, except that the data of the first single shot is unavailable, we assume that the initial states in the subsequent experiments are consistent with those in the random circuit sampling experiment.

Due to the influence of the fact that the final states in the random circuit are not all 0, we can observe that the state $|00\ldots0\rangle$ preparation fidelity obtained with the final state in the random circuit experiment is slightly lower than that of obtained with the the final state in the standard readout fidelity benchmarking as shown in Fig. S6 (c). Therefore, we need to consider this correction factor when calculating the estimated fidelity.

As shown in Fig. 3 in the main text, after considering all the correction method mentioned above, the experiment and the prediction can match well.

III. RANDOM CIRCUIT SAMPLING OF 31-QUBIT 2-PATCH CIRCUIT

We have also implemented the 2-patch version of the circuits, scaling from 12 to 32 cycles with 31 qubits each, and computed the linear XEB fidelities for the respective output bitstrings. The estimated and experimental fidelities for both

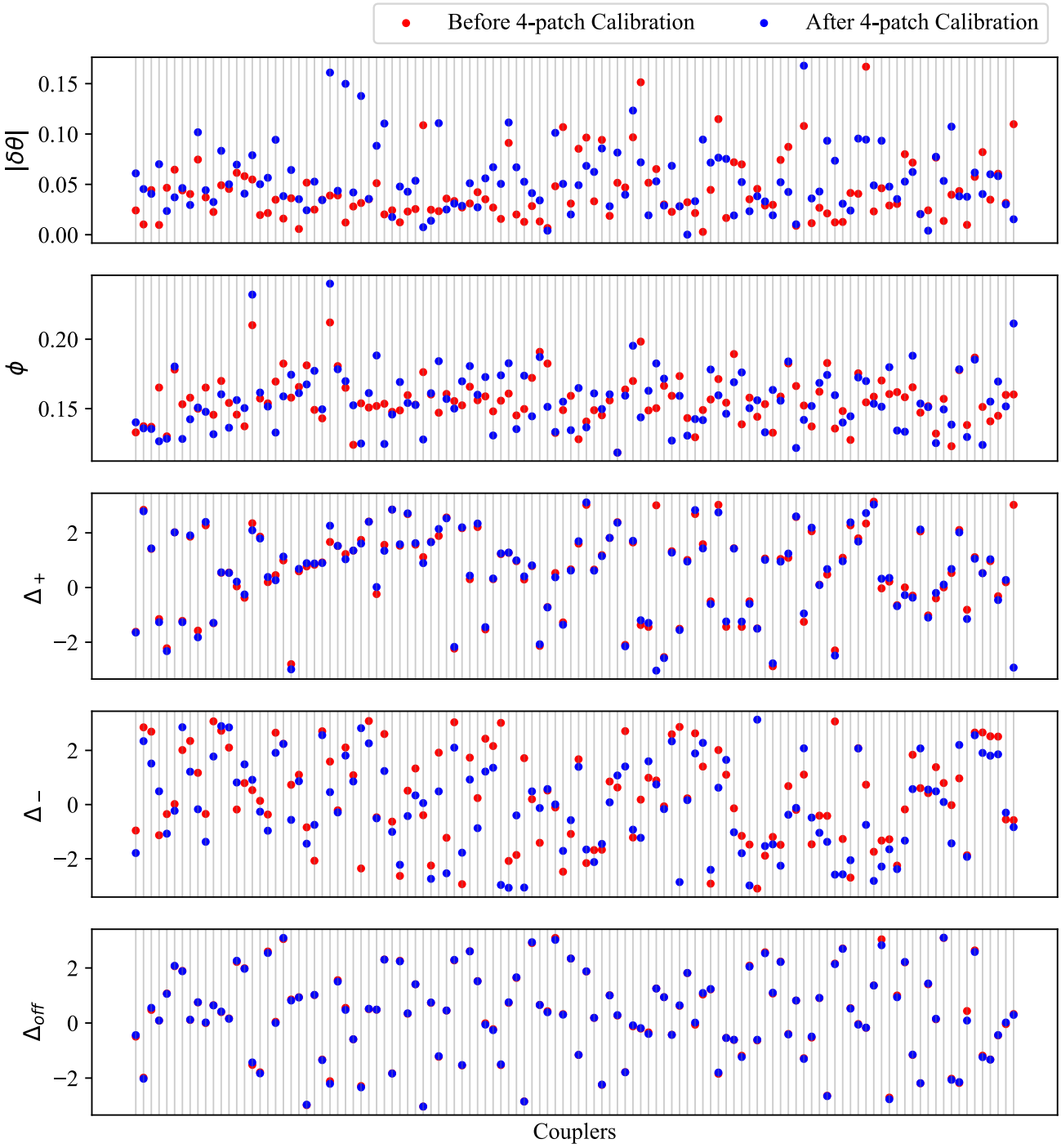

FIG. S5. **Comparison of the iSWAP-like gate parameters before and after 4-patch calibration in the Context of 83-qubit experiment.** The definitions of the five parameters in the figure can be found in Ref. [11]

the 2-patch circuits and the full circuits are depicted in Fig S7. The high degree of correspondence between the estimated and experimental results indicates that the discrete error model provides a reliable estimate of fidelity for both 2-patch circuits and full circuits when employing the 4-patch calibration method.

IV. RANDOM CIRCUIT SAMPLING OF 83-QUBIT FULL CIRCUIT

In the random circuit sampling experiment conducted on the 83-qubit, 32-cycle full circuit, we sample a total of 410 million bitstrings, a process that spanned 91 hours. To ascertain the reliability of our experimental setup, we insert ran-

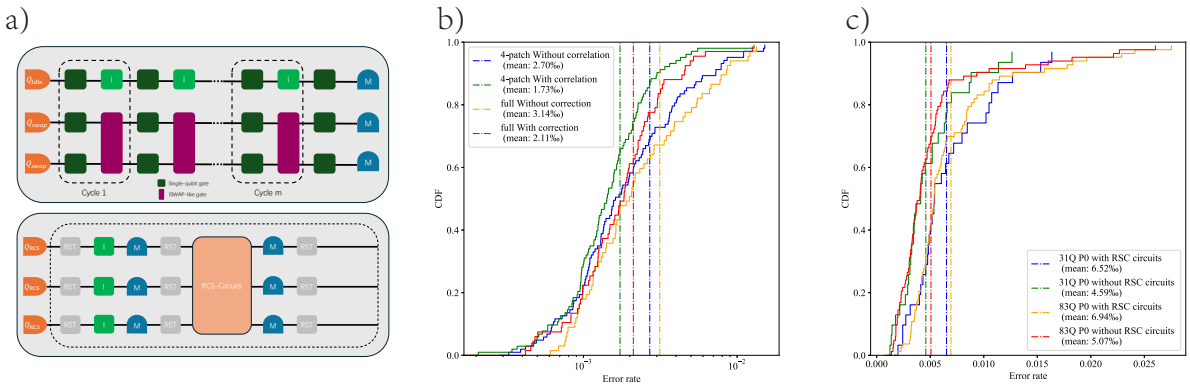

FIG. S6. **Extra error benchmarking in the RCS experiment. a)** Circuit diagrams for the benchmarking of the idle gate (top) and the readout error of P0 with RCS circuits (bottom). The single-qubit gates are chosen randomly from the set of $\sqrt{X}, \sqrt{Y}, \sqrt{W}$. **b)** CDF diagrams of the idle gate error with and without Z gate correction, in the 4-patch circuit and the full circuit respectively. **c)** CDF diagrams of P0 error with and without RCS-circuits, in 31-qubit and 83-qubit respectively. The vertical dotted lines in **b)** and **c)** represent the average value.

dom circuit sampling experiments before and after every 10 million bitstrings within the 83-qubit full circuit, sampling half a million bitstrings on the 83-qubit, 4-patch, 32-cycle circuit. Subsequently, we monitor the fidelity variation over time, as illustrated in Fig. S8. From the results of the 83-qubit 4-patch 32-cycle circuit, it can be seen that the XEB fidelity was within the range of plus or minus 25% of the estimated fidelity throughout the sampling period, which proves that our system had a sufficiently high fidelity and also verifies the validity of the data of the 83-qubit 32-cycle full circuit.

The computational complexity of random circuit sampling within an 83-qubit, 32-cycle system under various memory constraints is detailed in Table S2.

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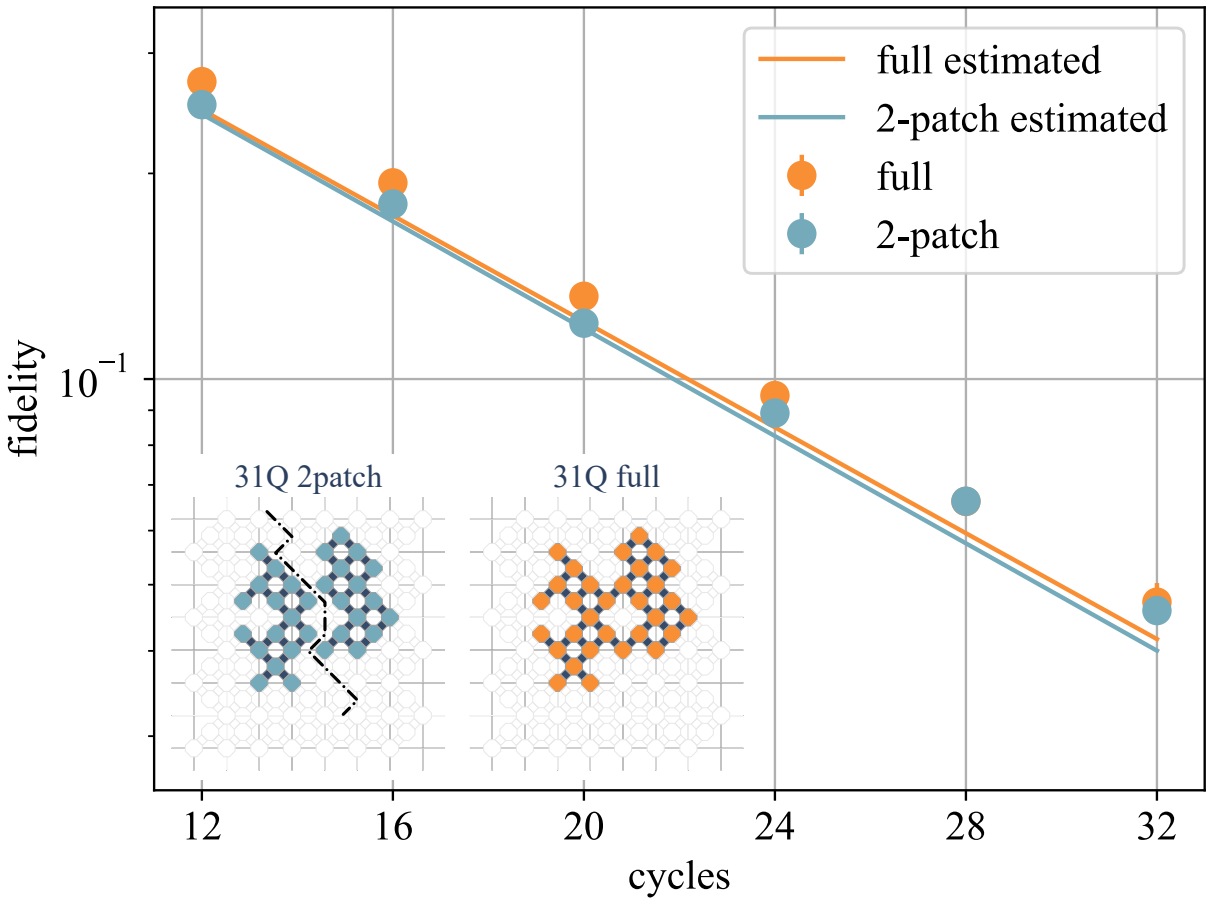

FIG. S7. **Experiment and estimate fidelity of random circuit sampling experiment for 31 qubits.** The green and blue dots respectively represent the experimental values of the 4-patch circuits and full circuits with 31 qubits over 12-36 cycles. The corresponding solid lines denote the estimated values for these circuits. The inserted topological diagram illustrates the specific configuration of 31 qubits.

TABLE S2. Complexity under different memory constraints

Experiment	**Fidelity**	**Memory Constraint: 9.2PB**		**Memory Constraint: 46.2PB**		**Memory Constraint: 762.2PB**	
		1 Amplitude	1 Million Noisy Samples	1 Amplitude	1 Million Noisy Samples	1 Amplitude	1 Million Noisy Samples
Sycamore-53-20	2.2×10^{-3}	7.2×10^{18}	6.5×10^{16}	9.5×10^{18}	5.9×10^{16}	5.9×10^{18}	6.1×10^{16}
Zuchongzhi-56-20	6.6×10^{-4}	9.3×10^{19}	2.2×10^{17}	9.0×10^{19}	1.8×10^{17}	1.0×10^{20}	1.5×10^{17}
Zuchongzhi-60-24	3.7×10^{-4}	3.2×10^{21}	1.6×10^{19}	3.0×10^{21}	1.0×10^{19}	3.0×10^{21}	2.3×10^{18}
Sycamore-70-24	1.7×10^{-3}	1.7×10^{25}	8.2×10^{25}	4.1×10^{24}	1.3×10^{25}	3.2×10^{24}	1.4×10^{24}
Sycamore-67-32	1.5×10^{-3}	8.2×10^{28}	4.7×10^{27}	3.9×10^{27}	2.6×10^{26}	1.3×10^{26}	9.6×10^{24}
Zuchongzhi-83-32	2.5×10^{-4}	5.1×10^{31}	8.4×10^{33}	3.0×10^{30}	1.3×10^{32}	1.3×10^{29}	7.5×10^{31}

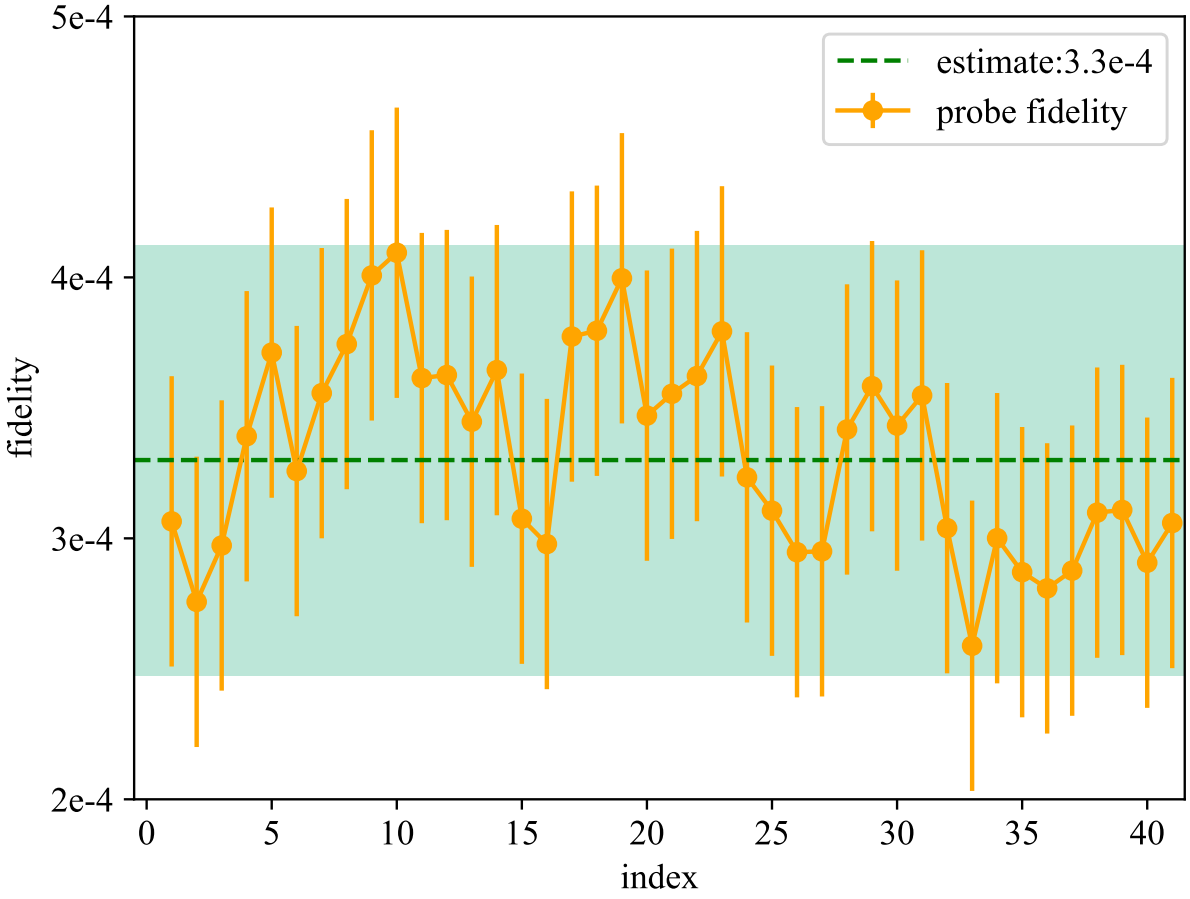

FIG. S8. **The fluctuation in probe fidelity over the course of the sampling process within the 83-qubit 32-cycle full circuit.** The dark green dotted line represents the estimated fidelity of 83-qubit 4-patch 32-cycle. The light green area indicates the range of plus or minus 25% of the estimated fidelity. The yellow dots represent the experimental fidelity of 83-qubit, 4-patch and 32-cycle with half a million sampling bitstrings throughout the entire sampling process, and each dot is approximately spaced 2.4 hours apart. It can be clearly seen that the experimental fidelity is within the light green area, demonstrating that our system is sufficiently stable during the sampling process.